In the Claims

1. (presently amended) A method used to etch a conductive layer to result in a selected profile of the conductive layer, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer;

forming a conductive layer over the semiconductor wafer~~;, wherein the conductive layer comprises~~

etching through the conductive layer to expose the semiconductor wafer substrate assembly on first and second sides of the conductive layer and to form first and second vertically-oriented cross-sectional sidewalls, each sidewall comprising a lower portion and an upper portion continuous with the lower portion, with the upper portion being further away from the wafer than the lower portion;

selecting a post-etch profile from ~~first, second, and third~~ first and second post-etch profiles, wherein:

~~the first post-etch profile results from an etch which removes lower and upper portions of each sidewall of the conductive layer at about the same rate to result in a substantially vertical profile of the conductive layer;~~

the ~~second~~ first post-etch profile results from an etch which removes the lower portion of each sidewall of the conductive layer at a faster rate than it removes the upper portion to result in a substantially U-shaped profile of the conductive layer; and

the ~~third~~ second post-etch profile results from an etch which removes the lower portion of each sidewall of the conductive layer at a faster rate than it removes the upper portion to result in the conductive layer having a profile which tapers inward at a uniform rate from the upper sidewall portion to the lower sidewall portion; then

etching the conductive layer using an etch comprising a flow rate of between about ~~6~~ 9 sccm and about 12 sccm He-O_2 to result in the conductive layer having the selected post-etch profile,

~~wherein the He-O_2 flow rate is about 6 sccm to result in the conductive layer having the first profile;~~

wherein the He-O_2 flow rate is about 9 sccm to result in the conductive layer having the ~~second~~ first profile; and

wherein the He-O_2 flow rate is about 12 sccm to result in the conductive layer having the ~~third~~ second profile.

2. (previously presented) The method of claim 1 wherein the etch of the conductive layer further comprises:

a flow rate of 50 sccm HBr;

a flow rate of an additional 100 sccm He;

a bias power of 70 watts;

a TCP power of 350 watts; and

a pressure of 60 mTorr.

3. (original) The method of claim 1 further comprising forming a polysilicon layer during the formation of the conductive layer.

4. (presently amended) A method used during the formation of a semiconductor device, comprising:

providing a semiconductor wafer substrate assembly comprising a semiconductor wafer;

forming a blanket conductive layer over the semiconductor wafer;

forming a silicide layer on the conductive layer;

forming a dielectric layer on the silicide layer;

etching the dielectric layer, the silicide layer, and completely through the blanket conductive layer at locations uncovered by an etch mask to expose the semiconductor wafer substrate assembly on first and second sides of the conductive layer and to form first and second sidewalls, wherein each sidewall is defined by the conductive layer, the silicide layer, and the dielectric layer, and wherein a lower portion of ~~the~~ each conductive layer sidewall is closer to the semiconductor wafer than an upper portion of ~~the~~ each conductive layer sidewall;

selecting a post-etch profile from ~~first, second, and third~~ first and second post-etch profiles, wherein:

~~the first post-etch profile results from an etch which removes lower and upper portions of the conductive layer at about the same rate to result in a substantially vertical profile of the conductive layer;~~

the ~~second~~ first post-etch profile results from an etch which removes the lower portion of the conductive layer sidewall at a faster rate than it removes the upper portion of the conductive layer sidewall to result in a substantially U-shaped profile of the conductive layer; and

the ~~third~~ second post-etch profile results from an etch which removes the lower portion of the conductive layer sidewalls at a faster rate than it removes the upper portion of the conductive layer sidewalls to result in the conductive layer having a profile which tapers inward at a uniform rate from the upper sidewall portion to the lower sidewall portion; then

with the silicide layer on the conductive layer and the dielectric layer on the silicide layer, etching the conductive layer using an etch comprising a flow rate of between about ~~6~~ 9 sccm and about 12 sccm $He\text{-}O_2$ to result in the conductive layer having the selected post-etch profile,

~~wherein the $He\text{-}O_2$ flow rate is about 6 sccm to result in the conductive layer having the first profile;~~

wherein the $He\text{-}O_2$ flow rate is about 9 sccm to result in the conductive layer having the ~~second~~ first profile; and

wherein the $He\text{-}O_2$ flow rate is about 12 sccm to result in the conductive layer having the ~~third~~ second profile.

5. (previously presented) The method of claim 4 wherein the etch of the conductive layer further comprises:

a flow rate of 50 sccm HBr;

a flow rate of an additional 100 sccm He;

a bias power of 70 watts;

a TCP power of 350 watts; and

a pressure of 60 mTorr.

6. (presently amended) The method of claim ~~1~~ 4 wherein the conductive layer is polysilicon.

7. (original) The method of claim 6 wherein the dielectric layer is nitride.

8. (new) The method of claim 1 further comprising etching the conductive layer using an etch comprising a flow rate of about 6 sccm He-O_2 to form the first and second vertically-oriented cross-sectional sidewalls.

9. (new) The method of claim 4 further comprising etching the conductive layer using an etch comprising a flow rate of about 6 sccm He-O_2 to form the first and second sidewalls.